REMARKS

These remarks are in response to the Official Action mailed on February 12, 2004, for which a one-month extension is hereby requested. The Applicants thank the Examiner for indicating the allowability of claims 15 and 24. The Office Action rejected claims 1-14, 16-23, 25, and 26 under 35 U.S.C. 103(a) as being unpatentable over Kwamura et al. (U.S. patent number 5,576,759) in view of Shibata et al. (U.S. patent number 6,011,714), with additional secondary references invoked for some of the dependent claims. It is respectfully submitted that these rejections are not well founded and that all of the pending claims are allowable over prior art.

In its rejection of independent claims 1 and 18, the Office Action cites Figure 2 and its corresponding description of Kawamura to supply the main elements of the claims, with Shibata to provide the details of the "high density analog/multi-level memory". The Office Action is correct in that Kawamura shows a "Main Buffer Memory" 3 connected between its "Image Processing Unit" 1 and its "Compression and Expansion Unit" 5; however, Figure 2 also clearly shows an "A/D Converter Unit" 2 interposed between "Image Processing Unit" 1 and the "Main Buffer Memory" 3. All of Kawamura's teachings are directed at first digitizing the output of "Image Processing Unit" 1 before it is stored in "Main Buffer Memory" 3, as is seen in the cited portions of Kawamura's specification; for example, see column 4, lines 32-37: "... *digitized* image signals are then stored as image data in the main buffer memory ...", where the emphasis has been added. Kawamura neither teaches nor suggests the storage of data in analog form in its "Main Buffer Memory" 3; instead, this would require the restructure of the circuit shown there in Figure 2 and the removal of elements that explicitly form part its teachings.

Concerning Shibata, this reference presents circuits related to storing analog or multi-value data. The specific teaching of Shibata relate to methods of writing and reading data to a memory cell such as that shown there in Figure 1 as 103. Although the Summary, Preferred Embodiment, and Claim section of Shibata make reference to "cells" in the plural, all of the explanation is given in terms of the circuit of Figure 1, which presents only a single memory cell devoted to holding user data. In particular, Shibata has *no teachings* directed to a *high density* analog/multi-level memory. (The Office Action cites column 1, lines 27-32. This does refer to the amount of data that may be present in image data; however, this is taken as

motivation for use of analog or multi-valued data cells instead of digital memory cells. The actual teachings of Shibata are then directed at circuitry for use with an analog or multi-valued data such as cell 103 of Figure 1. There is no discussion of applying these to a "high density analog/multi-state memory".)

In whole, claim 1 reads:

> A digital imaging system comprising:
> an image sensor to convert an image into analog data;
> image processing and compression circuits; and
> *a high density analog/multi-level memory* coupled between said image sensor and said image processing and compression circuits to receive and temporarily *store* said image converted into *analog data* from said image sensor and subsequently *transmit said analog data* to said image processing and compression circuits.

As the added emphasis indicates, claim 1 requires that the image data converted into analog form is stored in the memory *as analog data*, whereas Kawamura explicitly teaches converting the image data into digital form using the "A/D Converter Unit" 2 of its Figure 2 prior to storing this data in the buffer memory 3. As also indicated by the added emphasis, this analog data is stored in a *high density* analog/multi-level memory, an element not found in either Shibata or Kawamura.

Consequently, it is believed that rejection of claim 1 under 35 U.S.C. 103(a) as being unpatentable over Kwamura in view of Shibata is not well founded and that claim 1 is allowable over the prior art. It is respectfully submitted the Office Action is improperly relying on hindsight gained from the present invention to combine a primary reference, whose teachings are contrary to what is found in claim 1, with a secondary reference lacking in the element for which it is cited. For any of these reasons, it believed that a *prima facie* case has not been made that the rejection of claim 1 should be withdrawn.

Concerning claim 18, this is believed allowable for many of the same reasons given above with respect to claim 1. More specifically, it contains the middle element of "subsequently storing said image converted into said electrical signals *as analog data*", where the emphasis is added. As discussed with respect to claim 1, this is respectfully submitted to be contrary to teachings of the cited references. Consequently, it is believed that rejection of claim 18 under 35 U.S.C. 103(a) as being unpatentable over Kwamura in view of Shibata is not well founded and should be withdrawn.

The other rejected claims are all dependent claims having either claim 1 or claim 18 as their base claim and are consequently believed allowable for this reason. These claims all recite additional limitation and many are believed further allowable based on these; however, to save on space, these will not, except for claim 2, be discussed further at this time.

Concerning claim 2, the Office Action admits that "both Kawamura and Shibata are silent with regard to the exact size of their respective memories." It is also the case that these references are silent with regard to the rate and duration of data transfer. The Office Action then continues:

> "The courts have held that 'where the general conditions of a claim are disclosed in the prior art, it is not inventive discover the optimum or workable range by routine experimentation.' *In re Aller*, 220 F.2D 454, 456, 105 USPQ 233, 235, (CCPA 1955)."

It is respectfully submitted that the Office Action is incorrectly applying this ruling to present situation. The relevant questions are discussed in section 2144.05 of the M.P.E.P.. With respect to the present situation, is not the case of something like where, say, the prior art disclosed a range of 1-5% and the claim specified 4% (or even "slightly above 5%"). Rather, here, the teachings of the cited reference of Shibata only generally refer to "cells" in the plural. There is no discussion of any sort of range of the amount of data that can be stored, much less any suggestion of a range of values that would suggest a memory storing "more than 50 Mbits of said data." Consequently, "the general conditions" of claim 2 are *not* disclosed and it is *not* a question of just discovering "the optimum or workable range" within a set of general conditions. Consequently, the Office Action has not made a *prima facie* case for the rejection of claim 2.

This is also the case with respect to data rate recited in claim 2. As far as can be determined, Shibata provides no discussion of receiving data at any rate, much less of receiving "data at a rate of greater than 10 Mbits/sec for more than 5 seconds". Consequently, this also is *not* a case of just discovering "the optimum or workable range". Consequently, with respect to this limitation of claim 2, the Office Action has also not made a *prima facie* case for the rejection.

For these reasons, claims 1-14, 16-23, 25, and 26 are believed allowable. Reconsideration of claims 1-14, 16-23, 25, and 26 is respectfully requested and an early indication of their allowability is earnestly solicited.

Respectfully submitted,

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